TURBOchannel; The Performance Interconnect (script)

NOTICE

Title Slide

The title slide is used to differentiate TURBOchannel from a traditional bus architecture. TURBOchannel is designed as an I/O Interconnect specifically to solve I/O problems.

Slide 1

*TURBOchannel is a Synchronous bus (meaning that the system and all of the options in it are running in the same time domain. It has a 32bit address/data path.

* It is an asymmetric I/O channel in the sense that while a system knows about all of the options installed in it, an option only sees the system and not any other option.
* Latency is, of course, a option implementation dependent issue. But, the design of TURBOchannel allows for a very low latency.
* The protocol is scalable in the sense that it can be designed as a good performer in an entry level system, or a very high througput in a high-end system.

Slide 2

* In comparison to other desktop workstation I/O interfaces, TURBOchannel is very fast. Including the pipelining of the DS5000/200 it is capable of 90MB/s on that platform. It is possible to acheive 87MB/s in situations where the software is controlling the DMA transaction.
* At 12 control signals (only 44 signal pins over-all), TURBOchannel ranks as the simplest workstation I/O interconnect.
* A simple translation of this item is that "PINS = MONEY". The more complex a signal protocol is, the more expensive it is to implement in terms of hardware.
* By the term "proven" we mean that TURBOchannel is not a white paper that is discussing performance. It is an established fact. Digital has acheived 90% of the architectural performance of the protocol with its first product offering (that being the DS5000/200). That product has been shipping since April of 1990. Compare that with the other protocols on slide 3.

* The sole documentation around the use of TURBOchannel is the Technology Transfer Agreement found at the beginning of the specification. It makes the protocol available to both Option and System vendors completely free of charge.

Slide 3

* The table on this slide is comprised of the best performance information that was available at the time of composition. The restrictions on the information is that it is a comparison of shippable desktop workstation interconnects that are available as of the publication date of March of 1992. Only Public Specificaitons or Industry Standard interconnects are used for this comparison. The intent is that the interconnect must be open to the end user and to Option vendors. Private I/O interconnects (eg. a private graphics interconnect) are not considered.
* The Acheived DMA numbers are those available in public documentation. Any information correction should be sent to triadd@pa.dec.com for update.
* The interface signal pins comprise both the control signal pins and the address and datapath pins.
* In power per slot the total wattage is represented. No attempt was made to offer a breakdown by individual voltage (although such information is available, it just wouldn't fit on a single page). While 45 watts is the maximum Supply Current that is allowed in section 6.2 of the EISA Technical Reference Manual, we are not aware of any workstation implementation that uses this. The only guaranteeed current according to that same section is 2.0A of +5V which yields 10Watts.
* For the discussion of primary board area, we have provided the square centimeter totals for the TURBOchannel single slot profile (as all other characteristics are on a per-slot basis). However, it should be remembered that due to the clearance that is provided above the module, a mother-daughter card (or a SIMM assembly) are allowable. In the case of a mother-daughter card design like the DEFZA-AA, using double sided surface mount on the daughter card, you can acheive up to 504 sq. cm. of real estate for the design. In fact, the DECvideo option uses two such daughter cards in its design.
* Maximum Physical Address space is an architectural listing.

Slide 4

* The TURBOchannel is a synchronous protocol which can be run from 12.5MHz to 25MHz inclusive. Or potentially any point in between.
* The address and data-path are both 32 bit. But, they are time multiplexed. This means that the same signal pins are used to transmit both the address of the transaction and the data of the transaction itself.
* Only 44 signal pins (including both control signals and address/data).
* The board size provided is for a single slot option and (as in the previous slide) is only the primary board area.
* The specification allows for the design of single, double or triple width options. So in addition to the clearance above the option, you can also make them wider. The PXG+ and the PXG-TURBO+ are examples of these types of designs.
* The connector is a standard DIN type.
* Power supplied is additive accross option width. So, a triple width option like the PXG-TURBO+ has a total of 60Watts of power in +5V and 18Watts of +12V.
* TURBOchannel is one of the few I/O protocols which specifies the use of cooling air. One of the most common questions asked is why we provide so much power and cooling air. The answer is simple; interesting, high-performance logic has a cost in power (whether you are talking about using something like an Intel i860 processor, or just a lot of DRAM or VRAM) to operate, and likewise a cost in cooling to dissapate that same power. Enclosure designs which use only turbulent air flow (moving air around inside the enclosure but not exhausting the heat) or only convection cooling (depending upon the fact that hot air rises and providing no active air movement) are insufficient for the types of high speed, intelligent silicon that is used in today’s performance machines. Anybody can build an 8 line asynch option that doesn’t require much power, real-estate, or cooling air. But, try and design a 3D graphics accelerator, using an i860 coprocessor, 24MB of video memory, three rendering engine ASICs and three VDACs on just 30Watts and no active volume cooling air.

Slide 5

* The left hand diagram gives the outline of the single slot option module.
* The right hand diagram provides a cross-sectional view of the single slot option module. Note that the bulkhead would be to the left of this diagram with the TURBOchannel DIN connector pictured to the right of it. The clearances both above and below the option module are pictured with dashed line boxes.

Slide 6

* This diagram depicts the type of low cost system implementation where the address/data path of TURBOchannel is also used for the Processor to Memory interconnect. This is, in fact, the type of implementation that is used on both the PDS5000/xx and the DS5000/1xx systems. The reason why the interconnect from the Processor to Memory is in a shadow box is because the treatment of the CTL signals in that segment is not strictly TURBOchannel.
* Note that in this implementation there are still radial CTL signals to the options for both DMA and PIO. By radial, we mean that each option has its own control signals.

Slide 7

* This diagram outlines the intermediate implementation of a system. It provides a reasonable trade-off between cost and performance. We still see the use of a bussed address/data path for the TURBOchannel, as well as the radial control signals for DMA and PIO. But, we see a separate data path for the Processor to Memory interconnect. However, the Memory controller in this case is still one that implements time multiplexing. This is the type of implementation currently in use on the DS5000/2xx series machines.

Slide 8

* This diagram provides one variation of a high performance implementation of the TURBOchannel. We see here an implementation where each of the I/O Options has its own logical TURBOchannel (no bussed address/data path). As well, we see the possibility of a memory controller that will allow simultaneous access to system memory by the separate logical TURBOchannels. This would provide a system where the aggregate bandwidth of the I/O would be equivalent to the number of TURBOchannels in the system. It would not be easy (if possible) to do this for a general purpose system bus where the arbitration schemes are dependent upon bussed control signals.

Slide 9

* This diagram is a representation of a presentation that was made at the first TURBOchannel Industry Group session (the group which controls the migration and development of the TURBOchannel specifications and protocols). The idea is fairly simple. Since the TURBOchannel is based on a radial interconnect where each option is treated separately, we need not be concerned with responding to an individual option in a manner independent of the other option modules. The base system design is a full radial implementation (meaning a separate address/data path as well as separate control signals) consisting of, in this case, three separate logical TURBOchannels. The process would look like this:

- The system powers up at a 25MHz clock rate.
- The system reads the Option ROM header for the Option on TURBOchannel #1 and determines that this option is capable of sustaining a clock rate of 50MHz.
- The system then selectively turns up the clock rate on that single TURBOchannel to 50MHz giving that particular option a 200MB/s datapath to system Memory.
- The remaining Options having a 25MHz entry in their Option ROM header file are left at a 25MHz clock rate (each having <u>only</u> a 100MB/s datapath to system Memory.

- In this fashion we maintain complete backwards compatibility with all existing TURBOchannel Options that are compliant to the current specifications. While at the same time providing a 2X increase in the architectural capability. This is not feasible to do with a general purpose system bus that requires that the control signals be bussed as well. And, it is a simpler and cheaper implementation than to double the data path.

Slide 10

* This diagram provides an overview of the TURBOchannel Extender box. The idea here is to be able to move 1 (one) TURBOchannel option from the system enclosure and put it into the Extender enclosure. Since the TURBOchannel specs stipulate that an Option can only draw signals from one Option slot this means a three slot Option like the PXG-TURBO+ can be moved to the Extender and free up the other two logical TURBOchannel slots for use with other TURBOchannel options (eg. FDDI, Ethernet, SCSI).
* Additionally, since most people like to get maximum utilization out of enclosures in their office area, the box is capable of holding up to three SCSI devices. Those can be two half height drives and one half height removable media option.

Slide 11

* This is a brief list of benefits of the TCI ASIC (the specification for which is now available on gatekeeper: pub/DEC/TriAdd for anonymous ftp). Its current design is intended for a 160 pin PQFP (Plastic Quad Flat Pack).

Slide 12

* This slide provides a more detailed listing of features to support both DMA and PIO (Direct Memory Access and Programed Input/Output).

Slide 13

* This slide clears up some of the more common mis-understandings about the technology of the TURBOchannel.

Slide 14

* This slide provides contact information for Digital's TRI/ADD Program. Please feel free to contact us either with follow-on questions about this presentation or with comments and corrections.